A common-mode voltage reduction PWM method for three-phase unidirectional rectifier

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Abstract— In the present paper, a pulse width modulation (PWM) method that enables common-mode noise reduction in three-phase, three-level Vienna rectifiers is presented, and the losses in this system are compared and analyzed in relation to those of existing PWM methods. The proposed common-mode voltage reduction PWM method increases the number of times of switching compared to existing space vector modulation methods. The PWM method enables common-mode voltage reduction, and it is introduced through simulations; the losses are compared with other approaches to demonstrate the usefulness of the proposed PWM method.

Keywords—Common-mode voltage, Vienna rectifier, PWM

I. INTRODUCTION

A three-phase pulse width modulation (PWM) rectifier is required to meet harmonic regulation such as IEC 61000-3-2, IEC 61000-3-12, or IEEE519. Generally, two-level PWM rectifier is used to meet the regulations. Recently, however three-level Vienna rectifier was considered as a PWM rectifier. In the three-level Vienna rectifier, it is easy to reduce the input current Total Harmonic Distortion(THD) compared with two-level PWM rectifier, because the THD of the output voltage of a three-level Vienna rectifier is lower than that of a two-level rectifier. Furthermore, the semiconductor power element exhibits half the voltage stress compared with two-level rectifier. Thus, commonly used MOS FET device with lower voltage stress can be employed and the material cost can be reduced compared with two-level PWM rectifier. This Vienna rectifier topology also has a great advantage in terms of high efficiency, which arises because of the low switching loss. Due to their high efficiency, Vienna rectifiers have been used in the field demanding high-reliability power supply applications[1].

A problem with the PWM rectifier, however, is that it can be a source of the common-mode noise problem, even if the three-level Vienna rectifier has low level common mode noise compared with the two-level PWM rectifier. This common-mode noise is caused by the variation of the common-mode voltage. This has a negative influence on the Electro Magnetic interference(EMI) problem [2]. This EMI problem worsens the communication connection or electronic circuit function via electromagnetic interference. To eliminate common-mode noise, an EMI filter circuit is required[3]. However, it is difficult to generate an appropriate design for the common-mode EMI filter because of the limited choice of a Y-cap; this choice is limited because the leakage current is increased when a large Y-cap is used. Furthermore, reducing the common-mode noise is extremely difficult in relation to the stray value of the filter circuit, because common-mode noise is generally high frequency. In addition, the material cost will increase when the filter circuits are used.

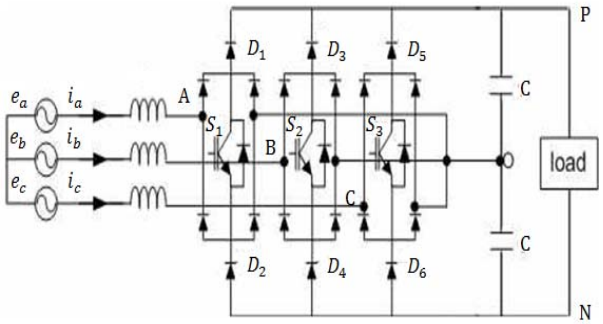

Fig. 1 A three-level Vienna rectifier circuit

To solve this common-mode problem, a method of reducing common mode voltage using the PWM technique for a three-level inverter is proposed.[4] This method employs a medium voltage vector which has no common mode voltage. However, in this paper, the method is only considered to apply to a three-level inverter, so it cannot be applied to directly to a three-level Vienna-type rectifier. In ref. [5], the carrier-based PWM method for a three-level Vienna rectifier was proposed to reduce common mode voltage. In that paper, common-mode noise reduction effects were demonstrated using this method. However, the switching events were increased for the proposed method compared to the conventional PWM method. Although this method had more switching events and the switching losses might be increased, however, there was mention of power device losses. In the present paper, the carrier comparison PWM method for common-mode reduction is reviewed in relation to conventional PWM methods and loss analysis moreover, PSIM simulation results are added. In the results of the loss comparison, it is clear that the losses do not

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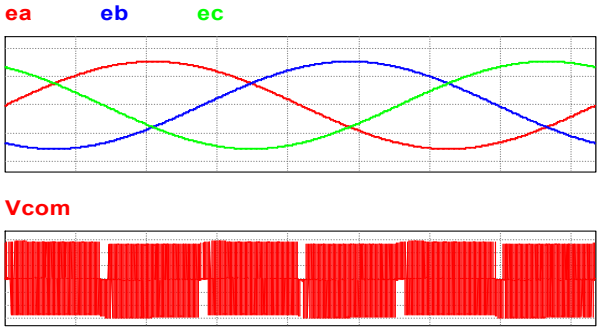
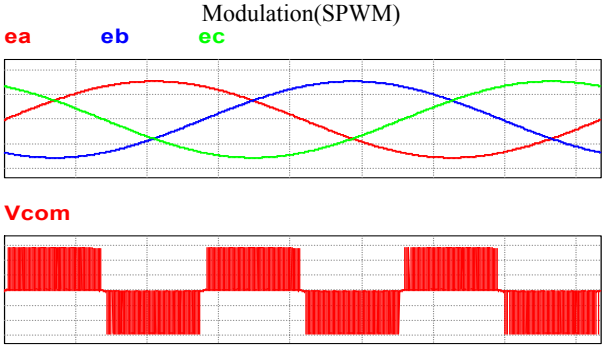


a. Common-mode voltage of Sinusoidal Pulse Width Modulation(SPWM)



b. Common-mode voltage of Space Vector Pulse Width modulation(SVPWM)

fig. 2. Common-mode voltages according to the three-level Vienna rectifier switching methods

increase although Medium Vector Pulse Width Modulation (MVPWM) method has the merit of common mode reduction.

II. PWM METHOD FOR VIENNA RECTIFIER

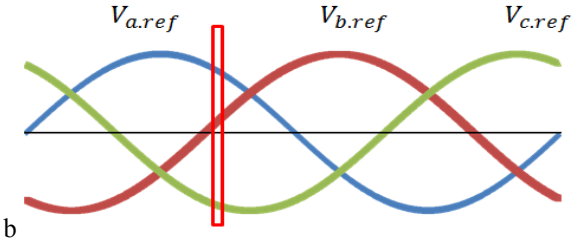
In Fig. 1, we can observe that the Vienna rectifier has a bidirectional switch with fast recovery diodes, one MOS FET switch, and two convention diodes in every phase. Here, ea, ev, and ec refer to the three phase system input voltages, and ia, ib, and ic refer to the three phase input currents. The output terminal voltages of Vienna rectifiers are depending on the on/off state of the bidirectional switch and the direction of the input current, and are described in the following. When S1, 2, and 3 are turned on, the terminal voltage of each phase comes to have a value of 0V; when S1, 2, and 3 are turned off, the terminal voltage will have a value of Vdc/2 if the value of the phase current is positive and a value of -Vdc/2 if the value of the phase current is negative.

A. Existing PWM methods

Figure 2 shows the common-mode voltage obtained using the existing PWM method of Vienna rectifiers. The equation for the common-mode voltage in the three-phase system is shown in Eq. (1), as follows:

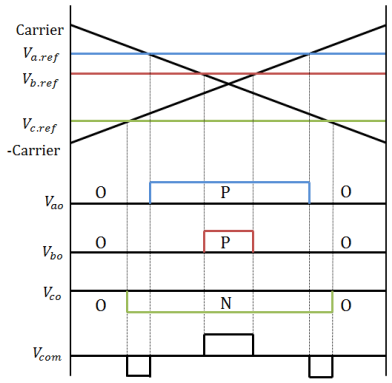
$$v_{com} = \frac{v_{a0} + v_{b0} + v_{c0}}{3} \qquad (1)$$

where v_{a0}, v_{b0}, v_{c0} refer to the output terminal voltages of individual phases, and v_{com} refers to the common-mode voltage. In addition, the relationship between the output



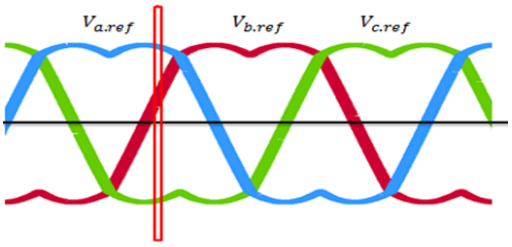
b

a. Reference voltage

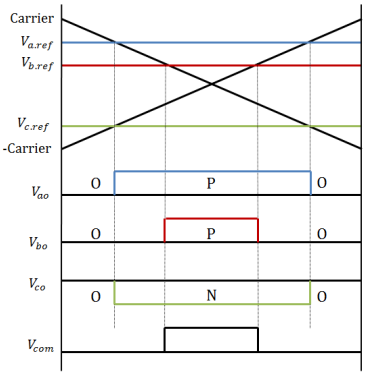


b. Common-mode voltage

Fig. 3. Common-mode voltage of SPWM



a. Reference voltage



b. Common-mode voltage

Fig. 4. Common-mode voltage of SVPWM

terminal voltage and the output phase voltage is shown by Eq. (2) in the case of SPWM and by Eq. (3) in for SVPWM.

$$v_{abc0} = v_{abcn} \tag{2}$$

$$v_{abc0} = v_{abcn} - \frac{\max(v_{abcn}) + \min(v_{abcn})}{2} \tag{3}$$

where v_{abc0} refers to the abc phase output terminal voltage and v_{abcn} refers to the abc phase output phase voltage. With regard to the output terminal voltage, on reviewing Fig. 2, it can be seen that the common-mode voltage decreases to approximately half in the case of SVPWM compared to that in SPWM. The reason for the difference in the common-mode voltage in the case of the existing PWM method is explained through Fig. 3 and Fig. 4.

Figure 3(a) shows the output terminal voltage reference of SPWM, and Fig. 3(b) shows the carrier comparison PWM process for the SPWM output terminal voltage reference and the resultant output terminal voltage and common-mode voltage determined through the process. Figure 4(a) shows the output terminal voltage reference of SVPWM, and Fig. 4(b) shows the carrier comparison PWM process and the resultant output terminal voltage and common mode voltage determined through the process. As shown in Fig. 3(b) and 4(b), the carriers are composed of two carriers—an upper carrier that operates when the terminal voltage reference is larger than 0 and a lower carrier that operates when the terminal voltage reference is smaller than 0. In the figure, "O" shows the state where the S1, S2, or S3 switch in Fig. 1 has been turned on so that the output terminal voltages of individual phases are connected to the intermediate point O and the terminal voltage becomes 0 [V]. P indicates the state where the terminal voltage reference is placed at (+) and MOS FET switches S1–S3 are turned off so that the upper diode is electrified and the terminal voltage becomes $0.5V_{dc}$; this is labelled "P." "N" indicates the state where the terminal voltage reference is placed at (-) and the switch is turned off, so that the lower diode is electrified and the terminal voltage becomes $-0.5V_{dc}$. Therefore, to review the common mode voltage using the terminal voltage obtained by comparing the reference voltage and the carrier for one cycle of the switching frequency, in the case of SVPWM, if three terminal voltages are added up, only one of (+) and (-) will appear on the basis of 0V during the switched cycle (Fig. 3). In contrast, in the case of SPWM, as shown in Fig. 4, both (+) and (-) will appear on the basis of 0V during the switched cycle. That is, it can be seen that common-mode voltage variations cannot but be larger in the case of SPWM than in the case of SVPWM.

This common mode noise can be a source of communication failure or measurement error. In addition, since the linear modulation of SVPWM is larger than that of SPWM by 12.2%, because the phase voltage of SVPWM is 90.7% and that of SPWM is 78.5% when compared to $0.5V_{dc}$, SVPWM is more advantageous than SPWM.

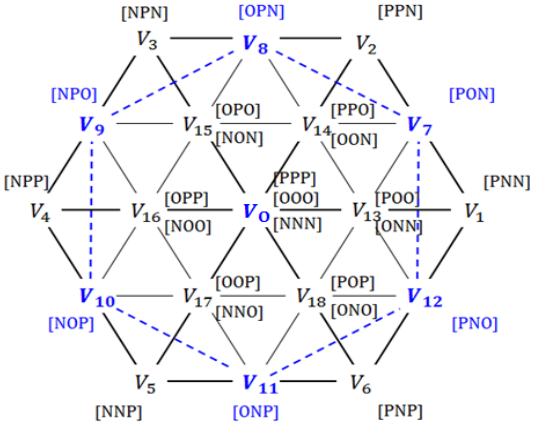
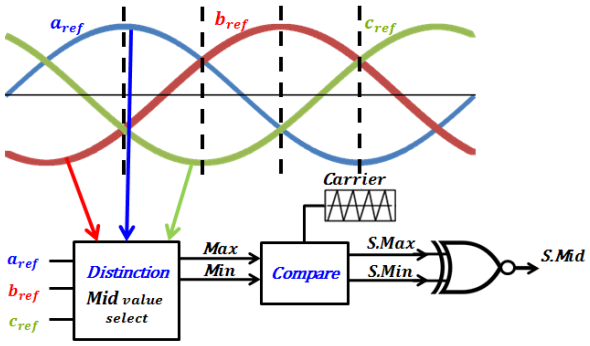


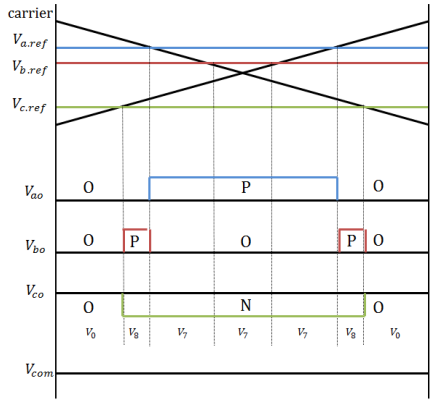
Fig. 5. Space vector diagram of three-3 level converter

B. *The PWM method for reduction of the common mode voltage for Vienna rectifiers[5]*

Figure 5 shows a space vector diagram of a 3-level converter[4,5]. If the space voltage vectors are classified according to their sizes, they are divided into three types—large vectors, medium vectors, and small vectors[4]. The common-mode voltage of V_1–V_6, which constitute large vectors, appears as $V_{dc}/6$, $(-V_{dc}/6)$. Meanwhile, the common mode voltage of V_{13}–V_{18}, which constitute small vectors, appears as $V_{dc}/3$, $V_{dc}/6$, and $(-V_{dc}/3)$,$(-V_{dc}/6)$. In contrast, the common mode voltage of V_7–V_{12}, which constitute medium vectors, appears as 0 [V]. Common-mode noises are generated in the case of existing switching methods because large vectors, medium vectors, and small vectors are used by turns. Figure 5 shows a diagram that expresses only medium vectors out of the three-level space vector diagram Figure 6 shows a carrier-based PWM method for reduction of the common-mode voltage of Vienna rectifiers. Since the method proposed in the present paper uses only medium vectors, the sum of the terminal voltages of three phases becomes 0, so that the common-mode voltage becomes 0 [V]. In Fig. 6, the a-phase reference, b-phase reference, and c-phase reference is set each of max, mid, and min, respectively. The switching function of the max phase and min phase is directly determined by the carrier comparison results. However, the mid phase voltage is determined by the combinational logic using the switching function of the max voltage phase and min voltage phase. The max-phase and min-phase comparison value added to the mid phase switching signal value equals zero. In the state of V_0, the A phase (max phase) reference voltage is less than the upper carrier signal, so the gate signal for S1 is 1. From the results, the A phase terminal voltage becomes 0 [V]. Furthermore, the C phase (min phase) reference voltage is greater than the lower carrier signal, so the gate signal for S3 is also 1. Thus, the C phase terminal voltage becomes 0 [V]. The B phase (mid phase) gate signal becomes 1 by the exclusive NOR from the S1 and S3 gate signal, so the terminal voltage becomes 0 [V]. By Eq. (1), the common mode voltage is 0. In the state of V_8,



a. Reference voltage



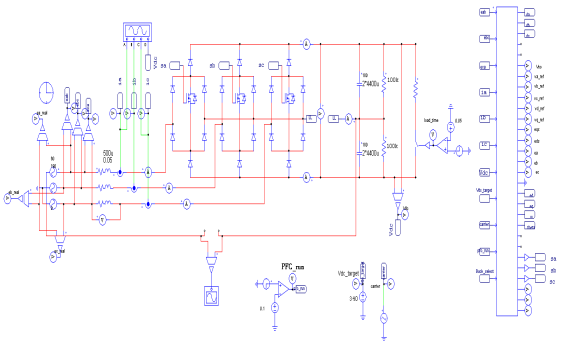
b. Common-mode voltage

Fig. 6. Common-mode voltage of the proposed PWM method

the A phase reference voltage remains lower value than the upper carrier signal, but the C phase voltage has a lower value than the lower carrier signal. Thus, the gate signal for S3 becomes 0, and the C phase terminal voltage becomes –0.5Vdc. For this reason, the gate drive signal for S2 is determined by the exclusive NOR function as 0, and the terminal voltage becomes 0.5Vdc. In this state, the common-mode voltage remains 0 [V] from Eq. (1). In the state of V_7, the A phase reference voltage is greater than the upper carrier signal. Thus, the gate drive signal is 0, and the terminal voltage of A phase becomes 0.5Vdc. By the exclusive NOR function, the gate drive signal of the B phase becomes 1, and the terminal voltage of the B phase becomes 0 [V]. In this state, the common-mode voltage also remains unchanged. In the results of the proposed PWM, the common-mode voltages are always 0 [V].

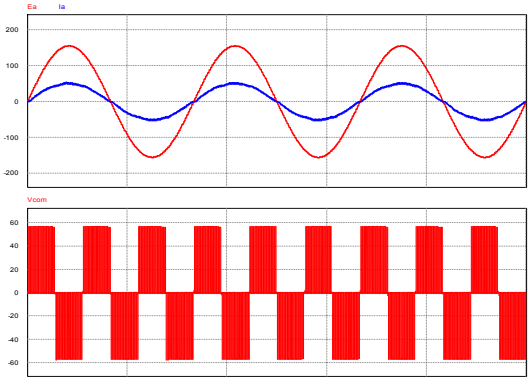
C. *Simulation Results and Experimental Results*

The parameters for simulation and experimentation are shown in Table 1. Figure 7(a) shows the simulation schematic. The simulation was carried out with PSIM. Figure 7(b) illustrates the simulation waveforms obtained while applying the conventional SVPWM, and Fig. 7(c) shows the simulation waveforms from the proposed carrier comparison PWM method. Figure 8(b) represents experimental waveforms from the conventional SVPWM, and Fig. 8(c) shows the experimental waveforms with the proposed PWM method. The conventional switching method generates a lot of common-mode voltage, while the proposed PWM method generates less voltage . This paper has demonstrated the effects of reducing

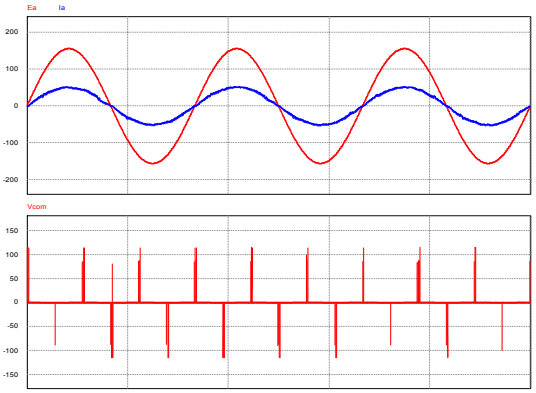


	Value
Intput RMS Voltage, Frequency	190[V_{rms}], 60[Hz]
Output Voltage	340 [V]
Power	2.1 [kW]
Switching Frequency	25 [kHz]
Input Inductor	0.5 [mH]

a. Simulation conditions

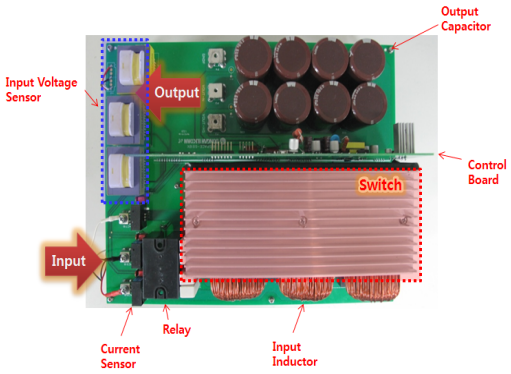


b. The SVPWM method

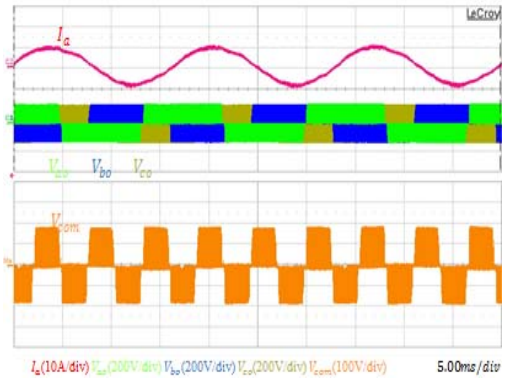


c. The Proposed PWM method

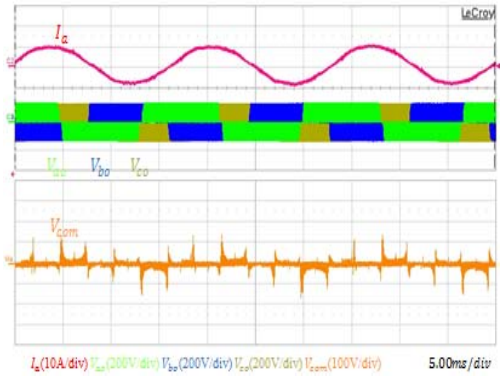
Fig. 7. Simulation results using PSIM



a. Experiments PCB



b. The SVPWM method



c. Proposed PWM method

Fig. 8. Experimental results

the variation of the common-mode voltage.

D. **Loss comparison**

The losses of the existing PWM methods and the proposed PWM method were analyzed through simulations. Figure 9 shows the switch losses according to load. From the results of the analysis, although the losses were not much different, the proposed PWM method and SPWM caused smaller losses, while SVPWM caused slightly larger losses.

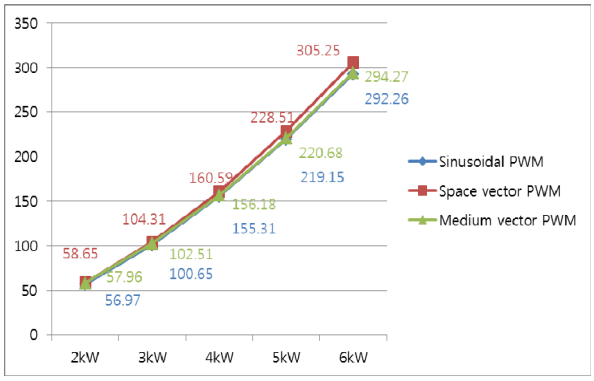


Fig. 9. Comparison of losses according to loads in the existing PWM method and the proposed PWM method

As explained above, a Vienna rectifier has a bidirectional switch consisting of two general rectification diodes per phase, four fast recovery diodes, and a MOSFET. Since the rectification diodes are always electrified in only one direction, they show little switching loss, while exhibiting some electrification losses that are relatively small because they are general rectification diodes. Therefore, most of the total losses are caused by the four fast recovery diodes and one MOSFET that constitute the bidirectional switch. To compare the terminal voltage references of SPWM and SVPWM, although the maximum voltage of SVPWM is lower, the time during which the maximum voltage remains is longer in SVPWM. Therefore, SVPWM comes to have more sections in which the switch is turned on than SPWM does. When the switch is turned on, the electrification loss of the switch may appear as i^2R due to the resistance component between the currents that flow though the switch and the drain and source. Since SVPWM has more sections in which the switch is turned on than SPWM, the electrification loss of the switch ($P_{con} = i^2R$) is shown to be larger in SVPWM than in SPWM. In the case of the proposed PWM method, among the three phase voltage references in SPWM, the mid value is generated by comparing the max value and the min value. Therefore, the proposed PWM method comes to switch the mid value once more compared to the existing SPWM. Therefore, the proposed PWM method has a larger number of instances of switching than SPWM, thereby causing slightly more switching losses. However, since the switching losses are relatively small because of the nature of MOSFET, the difference in the values is not large. In contrast, since SVPWM has a longer bidirectional switch electrification time compared to the proposed method, it causes relatively larger electrification losses.

III. Conclusion

The present paper proposed a switching method for reduction of the common-mode voltage occurring in Vienna rectifiers when SVPWM, which is an existing switching method, is used. The problem where sum of the terminal voltages of three phases does not become 0 could be solved by using the proposed PWM, which changed the switching of the mid phase to make the sum of the terminal voltages of three

phases into 0, thereby reducing common mode noises. Moreover, there was no difference in losses between the existing switching method and the proposed switching method. These differences were demonstrated through simulations.

REFERENCES

[1] B.-C. Yoon, H.-W. Kim, E.-Y. Cho, B.-K. Lim, "A single-carrier comparison PWM for voltage control of Vienna rectifier," Transactions of the Korean Institute of Power Electronics, Vol, 17, No. 2, pp. 129-134, Apr. 2012.

[2] M. Cacciato, A. Consoli, G. Scarcella, A. Testa, "Reduction of common mode currents in PWM inverter motor drives," IEEE IAS Annual Meeting, Vol. 1, pp. 707-713, 1997.

[3] M. Hartmann, H. Ertl, J. W. Kolar, "EMI filter design for high switching frequency three-phase/level PWM rectifier systems," IEEE Trans. Power Electron.2010.

[4] N.-S. Choi, E.-C. Lee, K.-S. Ahn, "A carrier-based medium vector PWM strategy for three level inverters in transformerless photovoltaic systems," Conf. Record on ICPE 2015, Jun 1-6, Seoul, Korea.

[5] Dong-Hyun Lee, Won-il Choi, Chang-Pyo Hong, Hag-Wone Kim, Kwan-Yuhl Cho, "Carrier Comparison PWM method of Vienna Rectifier for Reduction of Common Mode Voltage", The Transactions of the Korean Institute of Power Electronics