Differential Mode (DM) Current Ripple EMI Noise Analysis for Three-phase Vienna Type Rectifiers

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***Abstract*— For a Vienna rectifier, the phase-leg's pulsating voltage is the source for the input current ripple and Electromagnetic Interference (EMI) noise. Double Fourier integral transform is commonly used to determine the harmonic spectrum of the phase-leg voltage so as to predict EMI noise. For three-phase, three-level rectifiers, like the Vienna rectifier, this process can be very cumbersome and can vary depending on the modulation scheme used. Moreover it doesn't give direct estimate of the current spectrum which is needed for filter design as the limits of noise current spectra are given in many EMI standards. Hence, for designing the filter for the DM noise, detailed analysis of the DM ripple current is very important. In this paper, the DM ripple current in Vienna type rectifiers using a dual stacked carrier based modulation scheme is investigated and the technique to predict the worst current ripple is developed. Based on this worst current ripple, the method of finding the attenuation requirements for EMI filter design is also described. Simulations were conducted to validate the worst current ripple predicted using the proposed technique.**

Index Terms*— *Vienna rectifier, EMI, DM ripple current, dual stacked carrier, worst current ripple.

I. INTRODUCTION

To determine EMI filter topology for a converter, determining filter attenuation requirement is a primary task. For the estimation of DM filter attenuation requirement, the frequency spectrum for DM voltages and currents are used in system design stage [1][12][13]. From the EMI spectrum the attenuation requirements for certain band of frequency is found and compared with an EMI standard i.e. DO-160, CISPR etc. [2]. Finding the Fourier spectrum of the three level, Pulse Width Modulated (PWM) rectifier is a complex task which commonly uses Double Fourier integral transform for the phase leg voltage [3],[4]. This task becomes more difficult when Space Vector Modulation (SVM) is used as in this case, the reference may not be sinusoidal [5]. Relationship between SVM and three phase carrier based PWM has been shown in [6]. In the Vienna rectifier's case, a method for implementing SVM using the carrier based technique has been presented [5]. Hence, the Vienna rectifiers DM current ripple can be analyzed based on this carrier based implementation. Moreover, as the DM current ripple is not constant throughout line cycle, detailed analysis of this ripple is very important to understand its nature and find the worst possible case to find the EMI filter attenuation requirements.

In this work detailed DM ripple current analysis of Vienna rectifier is conducted using equivalent circuits derived from its operation conditions. Based on the DM ripple analysis, the worst current ripple has been identified and calculated. In the Vienna rectifier's case the worst current ripple is the ripple with the maximum magnitude at the fixed switching frequency [1]. Investigating the worst current ripple is necessary to find the EMI filter attenuation requirements. In this paper the technique of identifying and calculating worst EMI spectrum for the EMI filter design of Vienna rectifiers is explored. Based on the estimated worst current spectrum, both the filter attenuation requirement and filter topology are investigated.

II. THE VIENNA RECTIFIER

In this section, the operation of Vienna rectifier is briefly described. The Vienna rectifier topology is shown in Fig. 1. It consists of three single-switch legs associated to each phase, Q_1, Q_2 and Q_3. These are four-quadrant switches. These three switches are controlled to ensure line current shaping at the input, DC voltage regulation and middle point (M in Fig. 1) voltage stabilization at the output.

The Vienna rectifier circuit can be described based on the polarity of the phase currents (i_A, i_B, i_C) and the switching states of Q1,Q2 and Q3. In Fig. 1, a specific case $i_A > 0$; $i_B < 0$; $i_C < 0$ is considered. In this particular case, Q1 is OFF and Q2, Q3 both are ON. Now, considering ON=1, OFF=0, this operation state can be written as, Q1Q2Q3=011. Here, i_A goes through D1; i_B and i_C returns through Q2 and Q3 respectively. Within this operation state (011), top dc link capacitor C_1 is charged.

In another state in Fig. 2, Q1 is ON, both Q2 and Q3are OFF (Q1Q2Q3=100). The phase current polarities are the same as in the previous case. Here, i_A goes through Q1; i_B and i_C returns through D2′, D3′. In this case, bottom capacitor C_2 is charged.

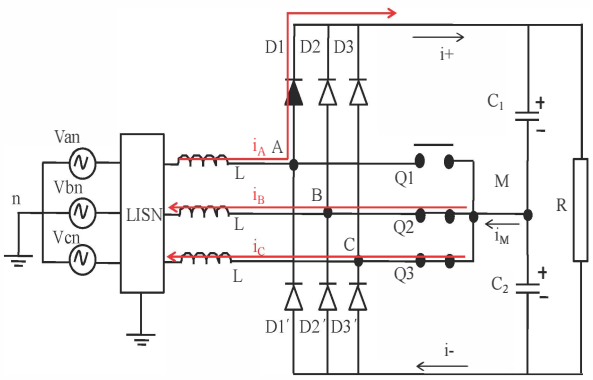


Fig. 1. The Vienna rectifier at the operating state 011.

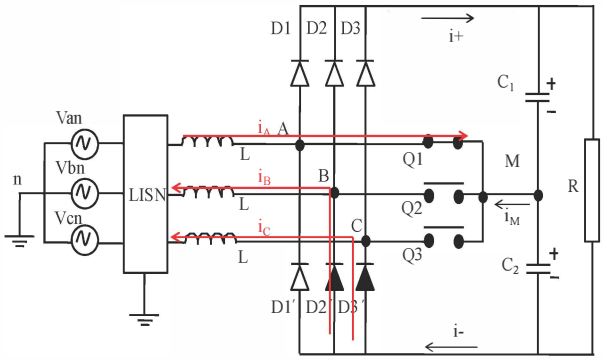


Fig. 2. The Vienna rectifier at the operating state 100.

It is shown that three switches of Vienna rectifier can have eight possible states as any switch can be either ON or OFF. But which of those states are present at a particular time instant depend on the modulation scheme. If a switch is ON, it connects the boost inductor L to the M point and if a switch is OFF the boost inductor is connected to the M point through a rectifier diode and the DC link capacitor. Depending on the direction of the current, based on this simple analysis and the substitution theory [10], there are two equivalent circuits for each current direction in each single phase. When the current through phase A, is positive the equivalent circuits are shown in Fig. 3. The V_{Mn} is the voltage between the midpoint of the DC link and the neutral point of the source and V_{an} is the input voltage for phase A. Following the same logic, when the current through phase A is negative, similar equivalent circuits where the current direction is opposite are shown in Fig. 4. Based on these equivalent circuits, DM noise ripple currents can be identified and calculated in the following sections.

III. Analysis of Input DM Noise Current

To find the DM ripple current for any phase, the single phase equivalent circuits as derived in the previous section is analyzed. Based on those circuits, V_{Mn}, and the duty cycle for the phase switches Q1, Q2, Q3 are needed for the analysis. The voltage V_{Mn} is dependent on the phase leg voltages, V_{AM}, V_{BM} and V_{CM}. If the voltage imbalance of the DC link capacitors is negligible and S_a is Q1's switching state (Sa=1, ON; Sa=0, OFF), V_{AM} can be written as [8],

$$V_{AM} = \frac{v_{dc}}{2}\mathrm{sgn}(i_A)(1-S_a) \tag{1}$$

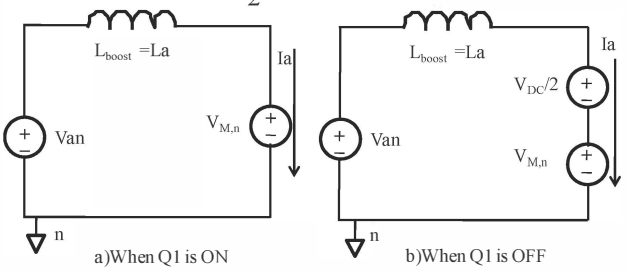


Fig. 3. Equivalent circuits when i_A>0 and switch Q1 is a) ON and b) OFF

V_{BM} and V_{CM} can be analyzed in a similar manner. Now assuming the input voltages are balanced sinusoidal functions,

$$\begin{aligned} V_{an} &= V_M \cos\omega t \\ V_{bn} &= V_M \cos(\omega t - 120°) \\ V_{cn} &= V_M \cos(\omega t + 120°) \end{aligned} \tag{2}$$

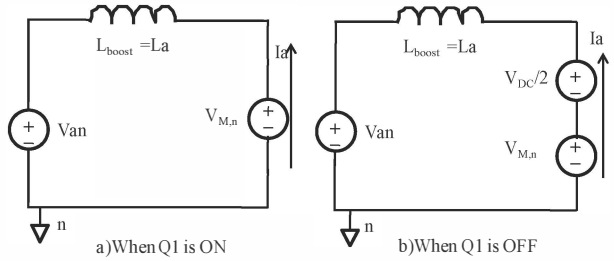


Fig. 4. Equivalent circuits when i_A<0 and switch Q1 is a) ON and b) OFF.

where, V_M is the peak value of the phase voltages. Using the expression for phase leg voltages, V_{Mn} can be written as [7],

$$\begin{aligned} V_{Mn} &= -\frac{1}{3}(V_{AM} + V_{BM} + V_{CM}) \\ &= -\frac{v_{DC}}{6}\sum_{k=a,b,c}\mathrm{sgn}(i_{sk})(1-s_k) \end{aligned} \tag{3}$$

Using (3), the V_{Mn} in different cases [7] can be computed. Different V_{Mn} values are calculated and listed in TABLE I. They are needed for ripple current calculation [7]. All possible line current polarities are considered here. It is to be noted that not all the switching states present in all the current magnitude and polarity conditions. Though the V_{Mn} for all the states in those conditions are shown here, only a few states actually occur (for reasons shown later based on the modulation scheme) and one or two states which hold for long time are sufficient to be considered for the ripple current analysis.

The third harmonic injection method is used in the modulation scheme [5], and hence, the voltage references of three phases are composed of voltages with fundamental frequency superposed with third order harmonics as shown in Fig. 5. For convenience of analysis, one full line period of three phase reference voltage is divided into twelve 30° sub periods based on the magnitude relationship of three phase voltage references as shown in Fig. 6. The reason behind the choice of 30° sub periods is that in each 30°, either the magnitude relationship or voltage directions of these voltage references changes. This affects the generation of switching state. For example, in section-1(0° to 30°) the relationship of the voltage references is, V_a reference > V_b reference > V_c reference; V_a reference is positive and the other two are negative. In section-2(30° to 60°), the magnitude relationship of the voltage references is still the same but both V_a reference and V_b references are positive; the V_c reference is still negative

Now, to find the ripple current, the expression for the duty cycle needs to be investigated. In this paper the duty cycle for phase leg A is named as D_a. D_a depends on the modulation scheme. The control of Vienna rectifier in this case, is considered to be a carrier based scheme [5], which is equivalent to space vector based control scheme but uses less computation. In this carrier based scheme, a dual stacked carrier is used for modulation. A reference voltage is compared with a dual stacked carrier to generate the duty cycle. Dual stacked carrier is used in three level rectifier modulation instead of single carrier based modulation which is used in two level rectifiers. Dual stacked carrier based modulation will be described below.

TABLE I
V_{MN} VALUES UNDER DIFFERENT OPERATION CONDITIONS

Conditions	Cosine Wave	V_{Mn} values for Switching states Sa,Sb,Sc							
	Degree	*111*	*110*	*101*	*011*	*100*	*001*	*010*	*000*
$I_a>0,I_b<0,I_c>0$	-90 to -30	0	$-V_{DC}/6$	$V_{DC}/6$	$-V_{DC}/6$	0	0	$-V_{DC}/3$	$-V_{DC}/6$
$I_a>0,I_b<0,I_c<0$	-30 to 30	0	$V_{DC}/6$	$V_{DC}/6$	$-V_{DC}/6$	$V_{DC}/3$	0	0	$V_{DC}/6$
$I_a>0,I_b>0,I_c<0$	30 to 90	0	$V_{DC}/6$	$-V_{DC}/6$	$-V_{DC}/6$	0	$-V_{DC}/3$	0	$V_{DC}/6$
$I_a<0,I_b>0,I_c<0$	90 to 150	0	$V_{DC}/6$	$-V_{DC}/6$	$V_{DC}/6$	0	0	$V_{DC}/3$	$V_{DC}/6$
$I_a<0,I_b>0,I_c>0$	150 to 210	0	$-V_{DC}/6$	$-V_{DC}/6$	$V_{DC}/6$	$-V_{DC}/3$	0	0	$-V_{DC}/6$
$I_a<0,I_b<0,I_c>0$	210 to 270	0	$-V_{DC}/6$	$V_{DC}/6$	$V_{DC}/6$	0	$V_{DC}/3$	0	$V_{DC}/6$

A. Dual Stacked Carrier

The comparison of single carrier and dual stacked carrier is shown in Fig. 7. Here, the carrier's frequency is considered to be much higher than the frequency of reference voltages, so the voltage references of three phases are almost constant within a carrier's period. The single carrier spans from -1 to +1. For the dual stacked carrier, because there are two carriers, one span from 0 to +1 and other spans from -1 to 0.

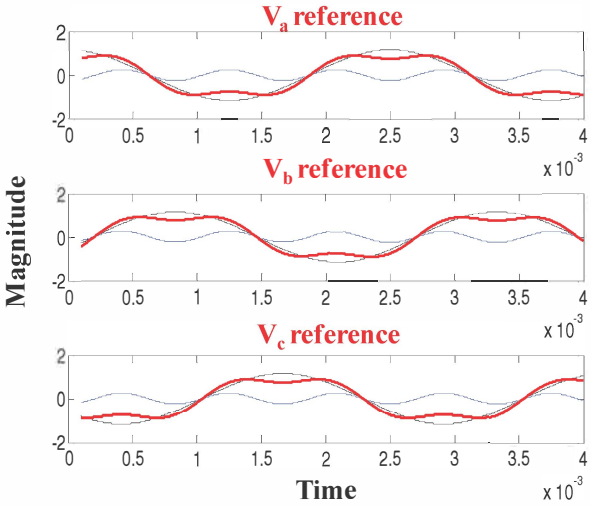


Fig. 5. V_a, V_b and V_c references along with their sinusoidal components and third harmonic components.

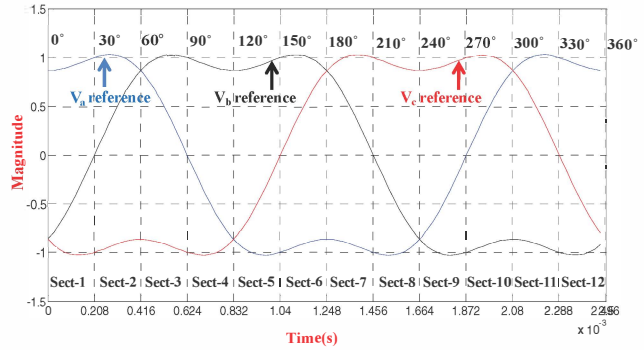


Fig. 6. One line period is divided into 12 30° sub periods for ripple analysis.

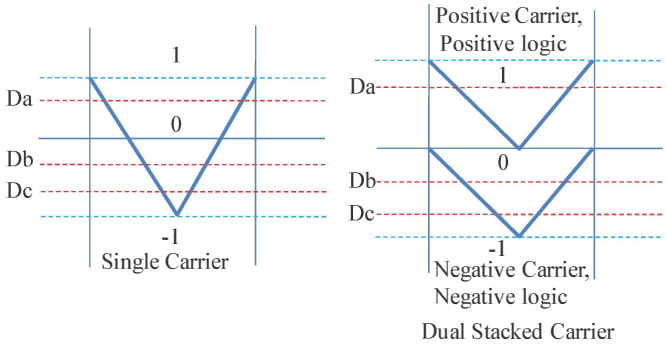
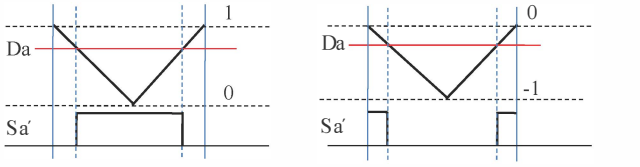


Fig. 7. Comparison of single carrier and dual stacked carrier.

The positive carrier uses a positive logic, which means if the reference is greater than the carrier then the duty cycle of a phase leg is positive and if it is less than the carrier then the duty cycle of that phase leg is zero. The negative carrier uses negative logic which is exactly opposite. This is shown in detail in Fig. 8. In Fig. 8, Sa′=1-Sa and Sa is the switching state of phase A's switch Q1. From Fig. 8, for the negative half cycle of the reference waveform, negative logic and negative carrier is used. If the absolute value of the reference waveform and the absolute value of the carrier are compared with positive logic, the generated duty cycle is same as that of negative carrier, negative logic. This equivalence is shown in Fig. 9. This equivalence is helpful for finding a common expression for the duty cycle for both positive and negative half of the line cycle. It is suggested that taking the absolute value of the duty cycle expression is necessary to find the ripple current in both the negative and positive halves of the reference waveform, as in that case the negative logic will not be dealt with.

An example of generating duty cycle with dual stacked carrier is shown in Fig. 10. Here, the reference signal, V_{ref} is constructed by adding a zero sequence component with the fundamental sinusoidal component. In the actual implementation, the frequency of the carrier is much higher than the frequency of the reference signal. Hence, the duty cycle, D_a is almost constant for one period of the carrier. D_a can be represented by the reference signal's expression. This carrier based generation of switching states to control the three

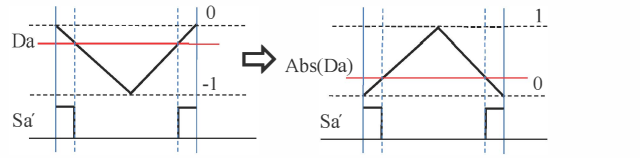
switches is equivalent to the space vector based method of generating the switching states [5].



a)Positive Carrier, Positive logic for +ve half cycle of reference

b)Negative Carrier, Negative logic, for -ve half cycle of reference

Fig. 8. Generation of duty cycle by a) positive and b) negative carrier



a)Negative Carrier, Negative logic

b)Absolute value of reference and Carrier, with Positive logic

Fig. 9. The equivalence of negative carrier, negative logic and taking absolute value of carrier with positive logic

In the carrier based implementation of the Space Vector Modulation (SVM) scheme, a zero sequence component is added to the reference signal to be in accordance with the SVM scheme. Hence, the duty cycle, D_a is constructed as, $D_a = D_a^{'} + d_0$, where, $D_a^{'} = \cos(\omega t)$, is the fundamental sinusoidal component of the duty cycle and d_0 is the zero sequence component. This d_0 has two parts as, $d_0 = d_0^{'} + \Delta d_0^{'}$. After simplifications, the first part, $d_0^{'}$ can be expressed as [8], $d_a^{'} = -\frac{1}{4}\cos(3\omega t)$. It is the reference for the injected third order harmonic. The other part of zero sequence, Δd_0 comes from the voltage imbalance in the two DC link capacitors and does not have a simple expression. Hence, the duty cycle expression finally becomes,

$$D_a = \cos(\omega t) - \frac{1}{4}\cos(3\omega t) + \Delta d_0 \qquad (4)$$

Δd_0 will be ignored due to its small magnitude in the following calculations. Neglecting it won't significantly affect the ripple current calculation.

B. *Analysis of Ripple Current at All Possible Regions*

To find the worst current ripple, one complete fundamental cycle of a single phase reference under all the possible conditions should be investigated. Phase A is taken as an example. As the Vienna rectifier works as a power factor correction converter, the input currents are in phase with input voltages. In each 30°, the relationship of currents and voltages of the three phases change accordingly. To find the ripple current, the reference voltages (similar to average duty cycle expression) is first compared with the dual stacked carrier in each 30° span of the reference and then the switch ON time as well as the switching sequences of all the three switches can be found. The switching state sequences are needed to find the V_{Mn} value as it varies depending on the switching states.

To find the worst current ripple, considering these 30° spans, one complete line cycle for a single phase has been investigated to find all the possible conditions. Based on this analysis for all the 30° spans, it is found that the maximum ripple occurs near some of the zero crossings of the reference voltages i.e. 60°-90°,90°-120°,240°-270° and 270°-300°. The analysis used for all 30° spans are similar to that shown in the next section for 90°-120° sector and this claim of the maximum ripple regions will be verified through analysis in the next section.

This theoretical analysis is also verified with a Vienna rectifier simulation as shown in Fig. 11. In the simulation, switching frequency is 20 kHz and the inductance of the boost inductor is 200µH. For brevity, only one maximum ripple region, 90°-120° span, is addressed here and the same method can be applied to other regions.

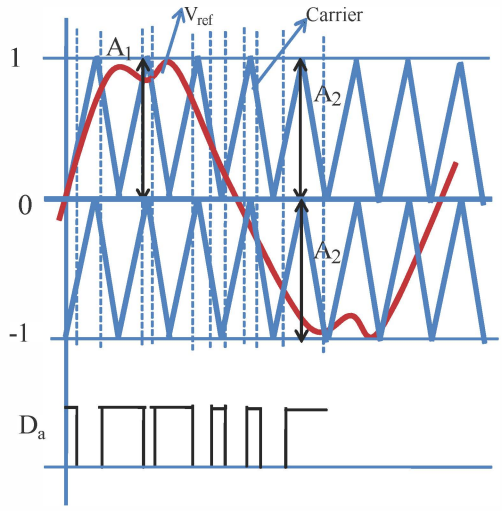


Fig. 10. Generation of the duty cycle to drive a switch.

C. *Ripple Current in the 90°-120° Span*

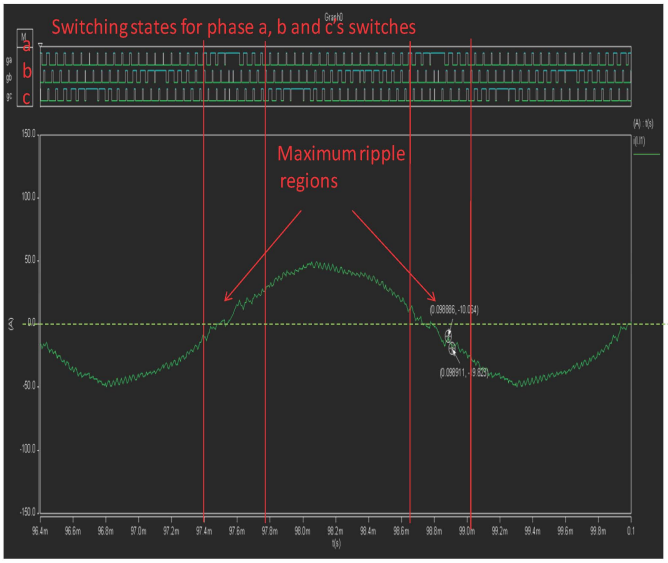


Fig.11. The maximum ripple current regions from Vienna Rectifier simulation for phase A's DM current along with the switching states for all the three phases.

Within 90°-120° span, comparing the reference with the dual stacked carrier, the switching states are sequentially generated: $S_aS_bS_c$= 010,000,100,101, as shown in Fig 12. To compute the current ripple, at first, state 100 is considered for the whole period as this state represents the ON time for switch Q1. The state 101 would be considered later to modify the computed ripple considering 100 state only.

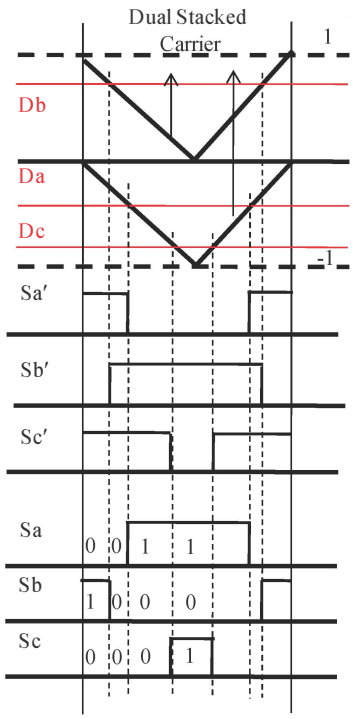


Fig. 12. Generation of switching states for 90°-120° region based on dual stacked carrier.

The DM ripple current equations can be derived from the equivalent single phase circuits of phase A in Figs. 3 and 4. When the phase current, $i_A>0$, the equation is,

$$\Delta i_A = \frac{(V_{an} - V_{Mn})T_s}{L}(1-|D_a|) \quad (5)$$

For $i_A<0$, this ripple current expression is,

$$\Delta i_A = \frac{(V_{Mn} - V_{an})T_s}{L}(1-|D_a|) \quad (6)$$

IV. Analysis of the Worst Current Ripple

In section III, with (5) and (6) and the switching state that holds for the longest time, the maximum possible current ripple throughout one line period can be calculated. The ripple current magnitudes for 0°-30°, 30°-60°,60°-90° and 90°-120° sectors are shown in Figs. 13, 14, 15 and 16. For brevity, the results of other eight sectors are not shown here. The parameters used in calculations are, $V_{an}(peak)=V_M=367$Volt, line frequency, $f_{line}=400$ Hz, DC bus voltage, $V_{DC}=700$Volt, boost inductor, L=100μH, switching frequency, fs=1/Ts=70kHz.

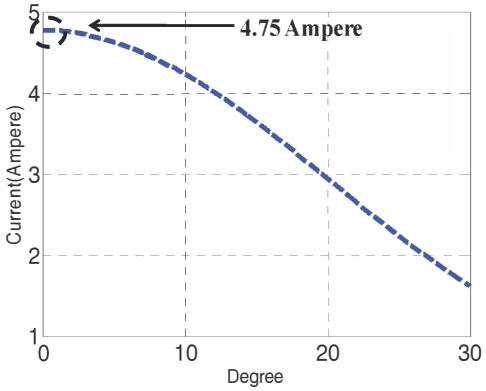


Fig. 13. Magnitudes of ripple current calculated between 0° and 30°.

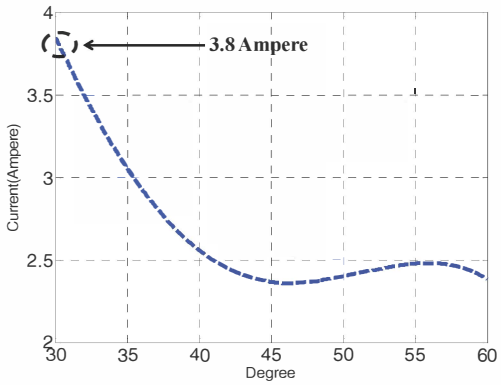


Fig. 14. Magnitudes of ripple current calculated between 30° and 60°.

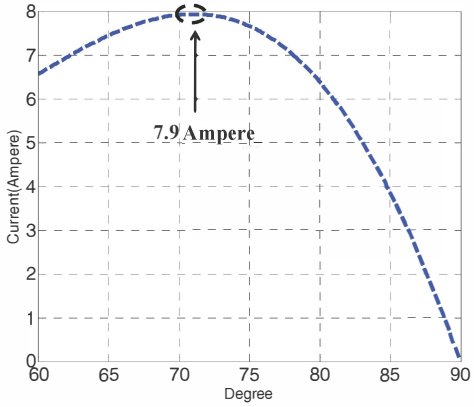


Fig. 15. Magnitudes of ripple current calculated between 60° and 90°.

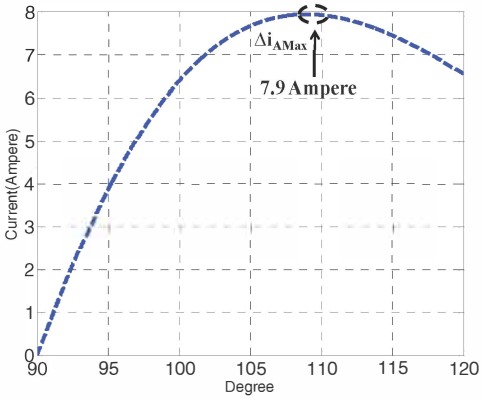


Fig. 16. Magnitudes of ripple current calculated between 90° and 120°.

As evident in (5), ripple currents are different at different instances of the line current waveform. Its magnitude depends on the variation of V_{an} and D_a. All possible states and the state which holds for the longest time in a switching period are considered in the analysis to obtain a close approximation of the original magnitude of the ripple current. The ripple current magnitudes in Figs. 13 to 16 constitute of discrete values calculated at corresponding angles using (5). It is shown from these Figs. that the maximum ripple magnitude is around 7.9 Ampere and it occurs both in 60°-90° and 90°-120° sectors. This result verifies the statement of the previous section that the maximum ripple regions occur near some of the zero crossings of the reference voltage i.e. 60°-90°,90°-120°,240°-270° and 270°-300°. Now, the continuous analysis is to be conducted within one of the maximum ripple region only (90°-120°).

In the 90°-120° sector, 100 state was investigated. The angle θ_{Max} at the maximum ripple is found from Fig. 16. With this information, duty cycle, D_a, at this maximum ripple can be found and based on this, the ON time for the switch Q1 is

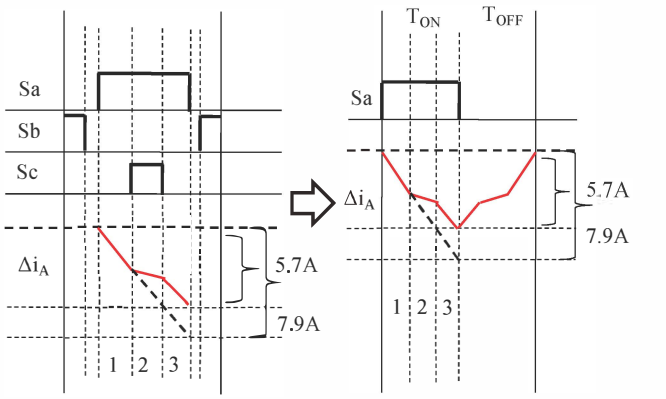
found as, $T_{ON1}=(1-|D_a|)\times T_s$. From Fig. 16, the angle θ_{Max} at the maximum ripple is 1.9 radian (109°). The duty cycle D_a at this maximum ripple is 0.533, which corresponds to an ON time for the switch Q1 as $T_{ON1}=0.467\times T_s$. To find the ON time for Q3(phase C switch), the duty cycle for phase C should be obtained, D_c. Now, as phase C is 120° leading to phase A, to find the duty cycle for phase C, D_c at this instant, the relationship [5] between phase A and C below is used,

$$D_c^{\theta_{Max}} = \cos(\theta_{Max}+\frac{2\pi}{3})-\frac{1}{4}\cos(3\times\theta_{Max}) \quad (7)$$

From (7), the absolute value of D_c is found as 0.8666, which gives the ON time for the switch Q3 (phase c switch) as, $T_{ON3}=(1-|D_c^{\theta Max}|)\times T_s=0.1334T_s$. The more accurate ripple current which is sequentially composed of currents of state 100,101 and again state 100(phase B's switch, Q2 is OFF in all these states and hence not considered in calculation). The following expression can be used to compute the more accurate modified ripple current,

$$\Delta i_{LA}=\frac{(V_{Mn1}-V_M\cos\theta_{Max})(T_{ON1}-T_{ON2})}{L}+\frac{(V_{Mn2}-V_M\cos\theta_{Max})(T_{ON2})}{L} \quad (8)$$

Here, V_{Mn1} is the computed value for state 100 and V_{Mn2} is the computed value for state 101. From this equation the modified maximum ripple current value is computed as 5.7 Ampere instead of the previously computed 7.9 Ampere. The modified ripple current is shown in Fig. 17(a). For the worst case consideration, in terms of both magnitude and harmonic content, the rising and falling edges are assumed to be symmetric, as shown in Fig. 17(b). In Fig. 18, phase A's current is zoomed in for 90°-120°, from the Vienna rectifier's simulation, using the same parameters as described previously. It is shown that the same shape and almost similar magnitude of 6.4 Ampere is found from the simulation. This is comparable to the analytical result as the rising and falling edges are not symmetric due to sinusoidal line frequency current wave shape on which the ripple is superposed.



a) Modified ripple current b) Ripple Current assuming falling and rising edge are similar

Fig. 17. a) Modified ripple current, b) ripple current showing both falling and rising edges.

V. Attenuation Requirements and Corner Frequencies of the EMI Filters Based on the Worst Current Ripple

In EMI filter design, EMI standards EMI need to be considered to calculate the attenuation requirements. In this work, the DO-160 specification is considered. The DO-160 specification starts at 150 kHz. Attenuation requirement is the maximum at low frequencies because the EMI spectrum of the current ripple in Fig. 18 decreases as frequency increases. The first harmonic of the rectifier, which falls in this range, will be explored for the worst case design. For the rectifier under investigation, the switching frequency is 70 kHz and its third order harmonic at 210kHz is the first harmonic falling within the concerned EMI range. The current ripple is not fixed and it changes based on line current and switching states. Hence to find the filter attenuation requirements, the worst current ripple needs to be investigated.

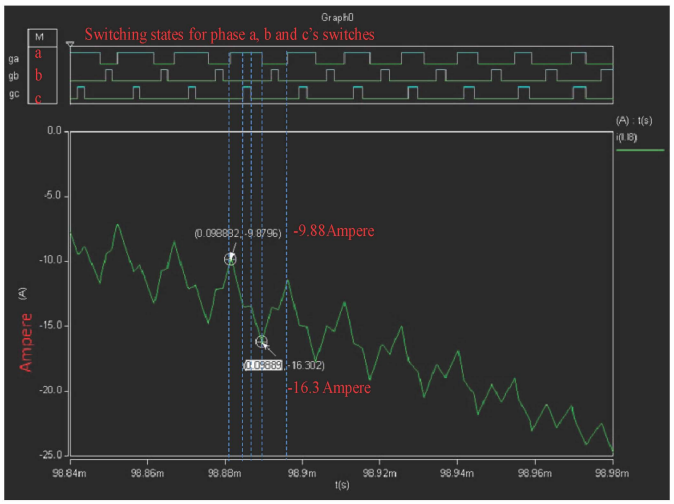


Fig. 18. The worst current ripple from the simulation of Vienna rectifier.

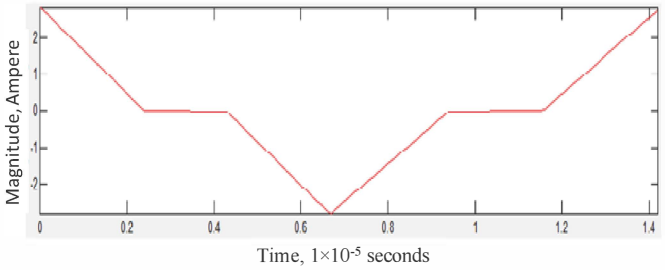


Fig. 19. Wave shape used for Fourier analysis.

Fourier analysis of the worst current ripple gives the worst possible third order harmonic. The Fourier analysis was conducted for the worst current ripple found in the previous section using MATLAB. The waveform under investigation for the Fourier analysis is shown in Fig. 19. The peak to peak magnitude is 5.8A. The symmetric shape, which is assumed in the previous section, is considered for Fourier analysis.

The Fourier spectrum of this waveform is shown in Fig. 20. Since this spectrum is the worst EMI spectrum and could be a little bit overestimated, it guarantees that the EMI filter designed based on it can meet EMI standards under all operation conditions. From the spectrum, the magnitude of the third order harmonic at 210kHz, is 0.68A. It is equal to 116.65 dBμA. For the DO-160 standard, the limit at 210kHz is 48dBμA. So the attenuation requirement at 210kHz is,

$$Att_{DM}=I_{DM_{(dB\mu A)}}-\text{Limit(DO160)}_{dB\mu A}+6dB \quad (9)$$

where, 6dB is a design margin and the required attenuation becomes, Att_{DM}=116.65-48+6=74.65dBμA at 210kHz. Based

on this attenuation requirement, filter corner frequency and topology can be determined.

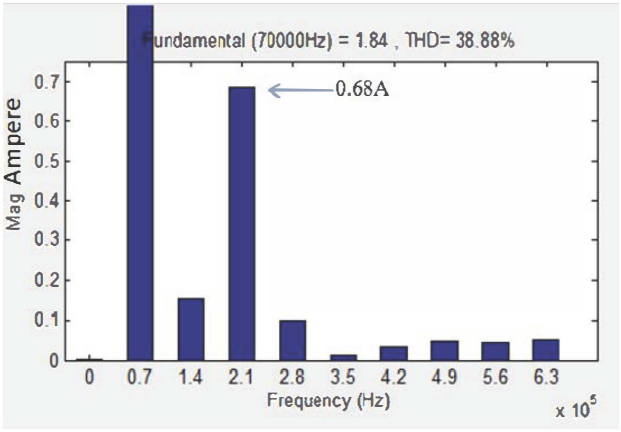


Fig. 20. Frequency spectrum of the worst current ripple in Fig. 19

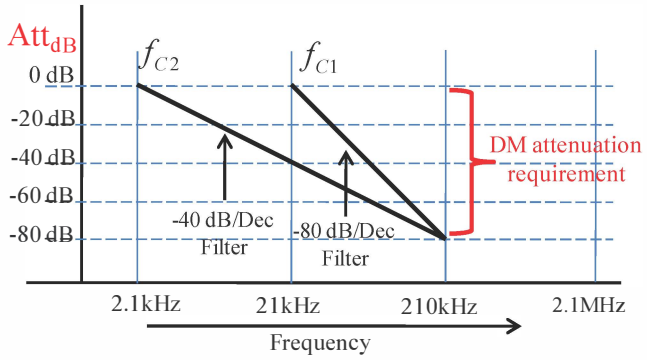


Fig. 21. Determining corner frequencies based on the attenuation requirements for a one-stage and a two-stage EMI filter.

The corner frequency design based on the attenuation requirement derived above for a one-stage LC filter and a two-stage LCLC filter is shown in Fig. 21. For the 2-stage LCLC filter with attenuation -80dB/Dec, the filter corner frequency f_{C1} is around 21kHz. For the one-stage LC filter with attenuation -40dB/Dec, the corner frequency f_{C2} is around 2.1kHz. Hence, the corner frequencies of desired EMI filters can be easily found to meet the attenuation requirements using the introduced worst ripple current prediction technique.

Besides the attenuation requirement, other factors such as the interactions [11] between power interconnects and EMI filter parasitics, and high power density [14] etc. should also be considered in final EMI filter design.

VI. CONCLUSION

In this paper, the technique to predict the worst current ripple is developed for three-phase Vienna type rectifiers. The equivalent DM ripple current models are developed. The current ripple is analyzed based on a double carrier based modulation scheme which is equivalent to SVM based scheme. The phase regions of the worst current ripples are identified. The magnitude of the worst current ripple is calculated. Simulations were conducted to validate the developed technique. The noise attenuation requirement is calculated based on the spectrum of the worst current ripple and EMI standards. The corner frequencies of one-stage and two-stage EMI filter are derived based on the attenuation requirement.

The technique of predicting the worst current ripple introduced in this paper can be applied to other rectifier or inverter topologies. It makes it possible to design a good EMI filter before the hardware is developed. It saves the time and reduces cost for EMI filter design.

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